Victory: Automatic Test Pattern Generation Tools (ATPG)

Automatic Test Pattern Generation Tools (known as VICTORY) are comprehensive set of software tools that are used to generate test-patterns and obtain diagnostic information for electronic assemblies containing boundary scan devices. The toolset also includes testability analysis tools for designing boards with boundary scan devices.

VICTORY was introduced in 1991, one year after IEEE adopted the 1149.1 boundary scan standard. Today, it remains the industry’s leading software for boundary scan design and test. More than 100 electronics manufacturers across the world are using VICTORY for boundary scan test generation.

VICTORY has four test pattern generation modules:

- Virtual Interconnect Test (VIT)
- Virtual Component and Cluster Test (VCCT)
- Boundary Functional Test (BFT)
- Boundary In-Circuit Test (BICT)

The boundary scan testability analysis module is called Access Analyzer (AA). Intelligent diagnostics is provided by the Boundary Scan Intelligent Diagnostic tool (BSID).
VIT module generates test patterns to detect faults in pure boundary scan interconnections. The VCCT module generates test patterns that determine defects in non-scan circuitry that is surrounded by boundary scan devices. VIT and VCCT tools also include a Test Access Port Integrity Test (TAPIT) module which is executed before other boundary scan tests to ensure that the Test Access Port (TAP) circuits of various devices on the chain are working properly. BSID isolates failures at the device, net, and pin levels. When defects cannot be identified in a deterministic manner, BSID provides intelligent messages that will point to probable sources of failure. AA is the module used for testability analysis and helps to reduce the number of test points on a DUT without diminishing fault coverage. BFT is used to test semiconductor devices complying with IEEE 1149.1 standard for defects in their core logic circuitry. If access via bed-of-nails is available to nodes on a target assembly, BICT patterns can be generated to test boundary scan devices resident on it. Typically, a combination of VICTORY modules is necessary to meet boundary scan test requirements and challenges. While VICTORY modules are offered on an individual basis, customers have been increasingly attracted to our bundled packages where they have been able to achieve significant savings in costs.
Virtual Interconnect Test (VIT)

The Virtual Interconnect Test (VIT) module generates patterns for testing boundary-scan nets using only the virtual access provided by boundary scan circuitry. VIT patterns provide 100% pin-level fault coverage for stuck-at pins, shorts, and opens.

On pure boundary-scan nets, VIT verifies that every device is operational at the pin level and that every interconnection – from silicon to lead bonds to solder bonds to the circuit board itself – is intact. VIT patterns can also verify the interconnections of an assembly's primary inputs and outputs, if physical test point access is available.

VIT Plus, a standard extension of the VIT module, supports in-circuit testing of assemblies that contain a mix of scan and non-scan logic. VIT Plus patterns provide 100% detection of shorts between boundary-scan nets and non-scan nets where only the non-scan nets have bed-of-nails access.

VIT and VIT Plus patterns are generated automatically from a circuit net list and the BSDL models of boundary-scan devices. VIT tests eliminate complex manual pattern generation, reduce the number of test pads required for detection of all structural faults, and simplify test hardware requirements.

VIT Features

- Detects stuck-at pin faults
- Tests shorts/opens
- Tests for shorts between scan and non-scan nets
- Tests transparent components (i.e. Buffers, Resistors)
- Implements logical constraints
- Provides detailed fault coverage reports

Defining Logical Constraints

VIT’s automatic pattern generator recognizes the logical constraints that users assign to the nets, leads, and tester pins involved in a VIT test. A logical constraint specifies the value that VIT will apply or detect for the duration of a VIT test. When an assembly has a mix of scan and non-scan devices, logical constraints are commonly specified to drive a net to constant logic state or to expect an un driven net to
remain at a constant logic state. This capability is used to disable or enable circuits that may be desirable or may interfere with a given test.

**Testing Transparent Series Components**

The VIT module can automatically generate patterns that propagate through transparent series components such as series resistors and non-inverting buffers, to test the continuity of their interconnections. For example, when VIT recognizes that there is a resistor in series between a boundary scan driver and receiver, it generates patterns that correctly test both nets by passing signals from the driver through the resistor to the receiver. Based on the information in the net list, device characteristic models, and user switches, VIT can automatically create an input file that identifies series components.

**VIT Fault Coverage Report**

The VIT module generates a fault coverage report to help test developers increase fault coverage on boards that have a mix of boundary scan and non-scan devices. In this report, all the nets on a DUT are sorted into six fault coverage classes. Each class defines the level of fault coverage that can be achieved using VIT, ranging from 100% fault coverage on pure boundary scan nets to zero fault coverage on non-scan-nets where there is no physical access. Using this report, test engineers can quickly see where other test techniques can be applied to improve fault coverage.

Network classes recognized by VIT:

- **Class 1**
  - Pure scan nets

- **Class 2**
  - Partial scan nets that have at least one scan driver, one scan receiver, and one non-scan device lead

- **Class 3**
  - Nets where scan outputs or tester channels drive non-scan inputs

- **Class 4**
  - Boundary-Scan inputs connected to power or ground

- **Class 5**
  - Non-scan nets with no tester access

- **Class 6**
  - TAP nets
One problem, that occurs frequently is, that scan and non-scan outputs are driving simultaneously in opposite directions Progressive vector generation through 6 classes of nets and related characteristic models keep developers in the driver’s seat, prevent contention, and device damage.

**Virtual Component /Cluster Test (VCCT)**

The VCCT module serializes parallel test patterns so that they can be applied through the boundary scan path to detect manufacturing faults on non-scan logic surrounded by boundary scan devices. VCCT can be used to test an individual non-scan component – such as a memory device – or a cluster of non-scan devices. VCCT can also apply a combination of serial and parallel test patterns to test the non-scan logic. When both serial and parallel test patterns are used, VCCT automatically synchronizes the application of serial patterns at scan cells with parallel patterns at the ParallelRiter™ card or tester channels.

VCCT patterns can also be applied through the ParallelRiter™ card to test and assembly’s I/O pins. VCCT uses the scan cells of boundary-scan devices as virtual channels to drive stimuli into the non-scan logic devices or clusters and detect responses from them. Stimulus patterns are conventional parallel test patterns which, VCCT regenerates into a serial format to apply via the boundary-scan path. Patterns for component test may be available from an in-circuit test library, a design pattern library, or they may have to be generated manually. VCCT testing includes the following capabilities:

- Detection of open and stuck-at faults on non-scan devices or clusters of non-scan devices using the scan chain
- Elimination of physical access requirements for testing conventional parts surrounded by boundary scan devices
- Automatic analysis to identify stimulus and measurement points for components
- Automatic serialization of parallel patterns to test non-scan devices or clusters
- Synchronous application of serial test patterns through the boundary-scan cells and parallel test patterns through the ParallelRiter™ card or in-circuit test channels
Boundary Functional Test (BFT)

BFT finds faults in internal device logic. The BFT module uses optional built-in test features available on some boundary scan devices to test internal device logic as part of an assembly or board-level test.

BFT is an effective test pattern generation tool for manufacturers who retest internal device logic as part of the assembly process and for repair depots responsible for isolating failures in the field.

Supports four techniques for internal testing of IEEE 1149.1 devices:

1. Functional test of the device TAP and scan register circuitry
2. Device logic test using the 1149.1 INTEST instruction

3. Device logic test using internal scan technology

4. Device logic test using the 1149.1 RUN BIST instruction
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